Abstract:

In this presentation we will discuss the challenges of chip-level verification of HBM and CDM events from GDSII layout for analog/mixed-signal, power management ICs and SOCs. ESD devices such as diodes, clamps and power clamps are modeled with TLP (for HBM) and vfTLP (for CDM) measurement data in the form of IV-curves, which may include snap-back behavior. HBM events are simulated statically (DC), while CDM events are simulated in transient mode due to the fast nature of CDM pulses in the 1-2ns range.

We will discuss the complexities of layout parasitic resistance extraction and model reduction in large chips, compare point-to-point with multi-point parasitic resistance extraction, ESD device modeling, very fast simulation techniques to deal with large number of tests in large chips, discuss trade-offs between static and dynamic (transient) simulation, compare simulation with rule based verification methodologies, discuss how to check for damage (voltage and current stress) in internal devices (in chip core and IO cells) including cross-power domain checks, charge sharing in CDM events, detect parasitic sneak paths through forward biased junctions and parasitic Bipolars, electromigration checks and IR-drops during an ESD event. In the second part, we will illustrate and demonstrate the above in Magwel’s ESDi (HBM) and CDMi (CDM) tools. We will conclude with future work.