

2019

台灣靜電放電防護技術論壇

Presenter: Dr. Dundar Dumlugol

Chairman and CEO of Magwel NV

Title: Simulation Based Chip-Level Verification Methodology of HBM and CDM Events



Abstract:

In this presentation we will discuss the challenges of chip-level verification of HBM and CDM events from GDSII layout for analog/mixed-signal, power management ICs and SOCs. ESD devices such as diodes, clamps and power clamps are modeled with TLP (for HBM) and vfTLP (for CDM) measurement data in the form of IV-curves, which may include snap-back behavior. HBM events are simulated statically (DC), while CDM events are simulated in transient mode due to the fast nature of CDM pulses in the 1-2ns range.

We will discuss the complexities of layout parasitic resistance extraction and model reduction in large chips, compare point-to-point with multi-point parasitic resistance extraction, ESD device modeling, very fast simulation techniques to deal with large number of tests in large chips, discuss trade-offs between static and dynamic (transient) simulation, compare simulation with rule based verification methodologies, discuss how to check for damage (voltage and current stress) in internal devices (in chip core and IO cells) including cross-power domain checks, charge sharing in CDM events, detect parasitic sneak paths through forward biased junctions and parasitic Bipolars, electromigration checks and IR-drops during an ESD event. In the second part, we will illustrate and demonstrate the above in Magwel's ESDi (HBM) and CDMi (CDM) tools. We will conclude with future work.

■ 時間:2019/7/16(二)13:30-16:30

■ 地點:新竹交通大學 交映樓(1F)國際會議廳

■ 參加費用:免費(請事先報名。因座位有限,額滿為止。)

■ 線上報名: http://www.alab.ee.nctu.edu.tw/~esd/reg.html

時間	課程與講師
13:30-14:00	報到 (Registration)
14:00-14:20	「 ESD產學聯盟」推廣說明 交通大學 柯明道 教授
14:20-16:00	ESD技術演講 Simulation Based Chip-Level Verification Methodology of HBM and CDM Events Dr. Dundar Dumlugol, Chairman and CEO of Magwel NV
16:00-16:20	Q & A

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